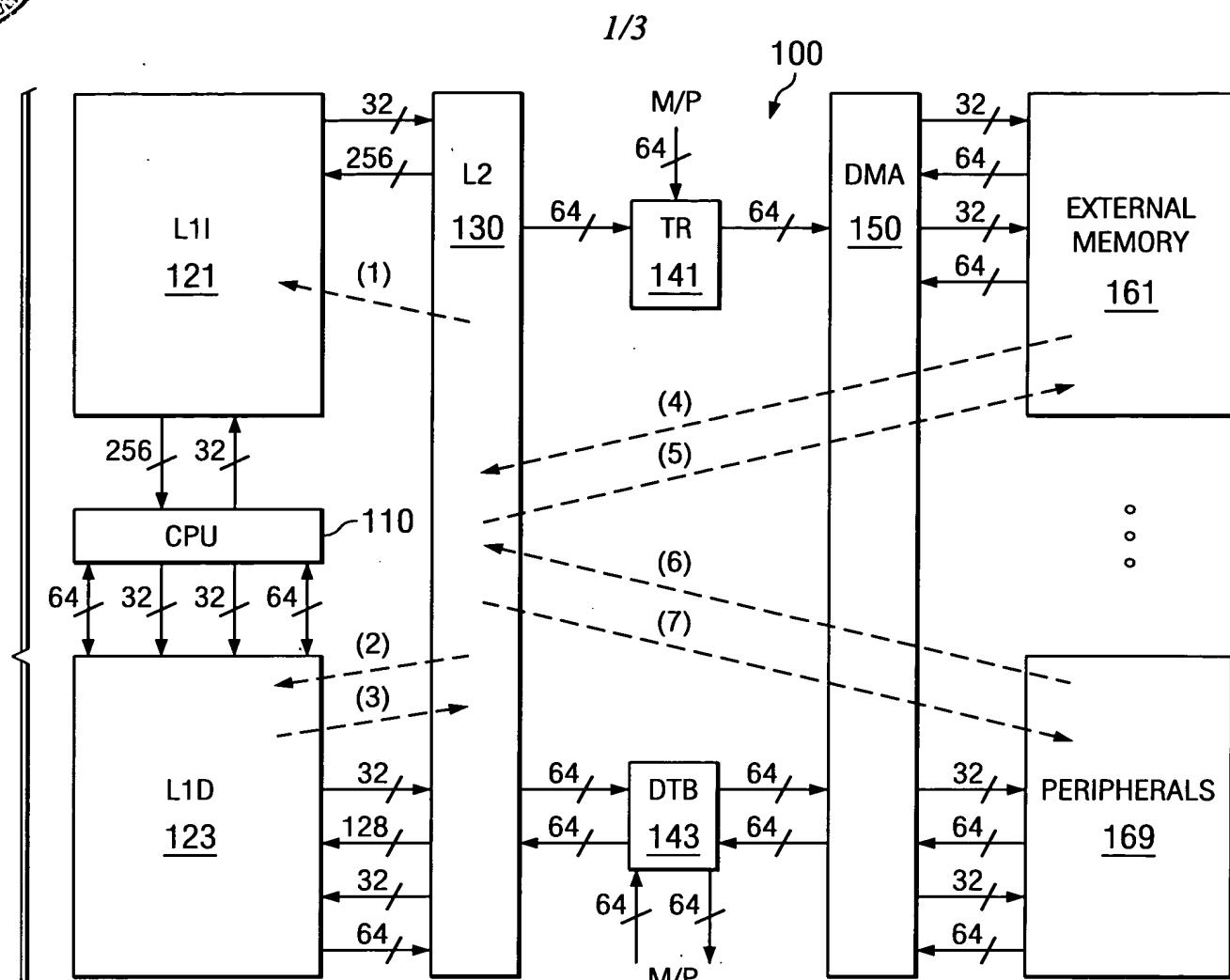




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- (1) L1I CACHE MISS FILL FROM L2
- (2) L1D CACHE MISS FILL FROM L2
- (3) L1D WRITE MISS TO L2, OR L1D VICTIM TO L2, OR L1D SNOOP RESPONSE TO L2
- (4) L2 CACHE MISS FILL, OR DMA INTO L2
- (5) L2 VICTIM WRITE BACK, OR DMA OUT OF L2
- (6) DMA INTO L2
- (7) DMA OUT OF L2

FIG. 1
(PRIOR ART)

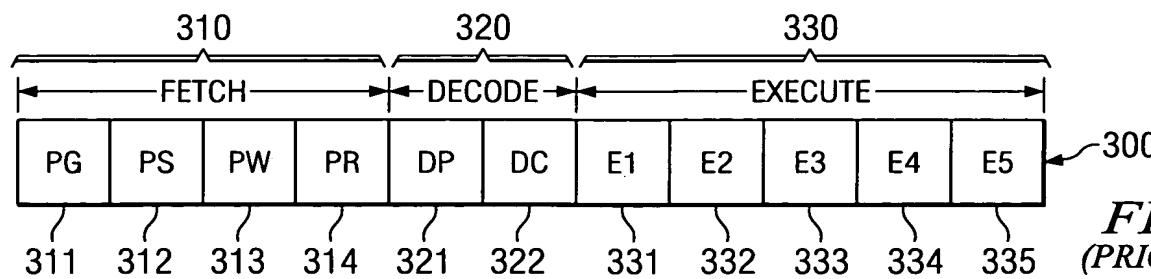


FIG. 3
(*PRIOR ART*)

FIG. 2
(PRIOR ART)

